REMARKS

The applicant has amended claims 1, 8, 15, and 17 to address potential statutory subject matter and indefiniteness issues. The applicant has also canceled claims 20-27 because after the previously noted amendments, these claims appeared to have not been substantially different than those already presented.

Applicant offers the following remarks regarding the outstanding rejections noted herein with respect to the amendments above. First, claims 1-27 stand rejected under 35 U.S.C. § 101 as being drawn to non-statutory subject matter. Specifically, the examiner indicates in the Action that the phrase "evolving a circuit" does not recite a useful object or result, and, therefore, claims an abstract idea. Applicant has amended the claims to indicate that the method is employed to design an electronic circuit. This should obviate these rejections.

Next, claims 1-27 stand rejected under 35 U.S.C. § 112, second paragraph as indefinite. Specifically, the examiner objects to the phrase "method of evolving a circuit" throughout the claims as indefinite because the type of circuit is unclear. Also, the language in the producing step in claims 1 and 18 is unclear as well as the language of claim 16.

Applicant has amended the claims to indicate that the method is drawn to designing an electronic circuit. Applicant has also amended the producing step in claims 1 and 18 with the language suggested by the examiner in the Action. Further, applicant has amended claim 16 with language similar to that provided by the examiner. These amendments should obviate all potentially unclear language so that the claims meet the requirements of the second paragraph of 35 U.S.C. § 112.

Finally, claims 15 and 17-20 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Stoica et al., "Evolutionary Design of Electronic Devices and Circuits, Evolutionary

Computation" IEEE CEC 99, July 1999 in view of Weste et al, "Principles of CMOS VLSI Design: A System Perspective," Second Edition, 1993, Addison-Wesley Publishing Company. Specifically, the examiner indicates that Stoica et al. teaches the general method of evolving a circuit and Weste et al. discloses running a homogenous mix of models of different resolutions. The examiner further indicates that combining these references to obtain the limitations would be obvious to one skilled in the art.

Applicant believes that the examiner has misconstrued the Weste et al. disclosure. Section 6.6.1.5 of Weste et al. discloses using different simulation logic on separate portions of an overall single circuit ("Each circuit ***block*** (bold/italic added for emphasis) can be simulated in the appropriate mode."—i.e. cell logic block in one mode, memory in another, etc.). The present invention runs iterative simulations on an entire circuit, each at a different resolution level. It is significantly different to run several simulations at different resolutions on an entire circuit design versus running several simulations on different portions or blocks of a single circuit. Applicant has amended the claim to more clearly identify these differences. Thus applicant believes that the current claims are not obvious over the current references.

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Accordingly, applicant believes that claims 1-27 are in condition for allowance and respectfully requests the examiner to withdraw all objections and rejections and allow said claims. Should the examiner need more information regarding this matter or have further suggestions regarding this application, feel free to call the undersigned at 818-354-7770.

Respectfully submitted,

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